CLAIMS

1. An alignment method comprising the following steps:

laying out a pattern representing a hexagonal arrangement of cMUT elements having axes of symmetry, said laid-out pattern comprising a first set of graphical data;

processing said first set of graphical data to rotate said pattern by a predetermined angle relative to a fixed rectilinear frame of reference having two mutually orthogonal axes, said predetermined angle being selected so that an axis of symmetry of said hexagonal arrangement of hexagonal cMUT elements is aligned with an axis of a first fixed rectilinear frame of reference;

laying out a first alignment key having an axis aligned with an axis of said fixed first rectilinear frame of reference, said laid-out alignment key comprising a second set of graphical data;

transferring said rotated pattern and said first alignment key to a mask; and

placing said mask over a substrate comprising a hexagonal arrangement of CMOS cells having axes of symmetry respectively aligned with the axes of a second fixed rectilinear frame of reference, and a second alignment key having an axis aligned with an axis of said second fixed rectilinear frame of reference, said mask being placed so that said first alignment key is aligned with said second alignment key.

2. The method as recited in claim 1, wherein each of said cMUT elements is hexagonal and each of said CMOS cells is rectangular.

3. An alignment method comprising the following steps:

laying out a pattern representing a hexagonal arrangement of cMUT elements having axes of symmetry, said laid-out pattern comprising a first set of graphical data;

laying out a first alignment key having an axis, said laid-out alignment key comprising a second set of graphical data;

processing said second set of graphical data to rotate said first alignment key by a predetermined angle relative to said axes of symmetry, said predetermined angle being selected so that said axis of said first alignment key is aligned with one of said axes of symmetry of said hexagonal arrangement of hexagonal cMUT elements;

transferring said pattern and said rotated first alignment key to a mask; and

placing said mask over a substrate comprising a hexagonal arrangement of CMOS cells having orthogonal axes of symmetry respectively aligned with the axes of a second fixed rectilinear frame of reference, and a second alignment key having an axis aligned with an axis of said second fixed rectilinear frame of reference, said mask being placed so that said first alignment key is aligned with said second alignment key.

4. The method as recited in claim 3, wherein each of said cMUT elements is hexagonal and each of said CMOS cells is rectangular.

5. An integrated circuit comprising:

a substrate comprising a hexagonal arrangement of CMOS cells; and

a hexagonal arrangement of micromachined elements,

wherein each micromachined element overlies a respective CMOS cell in one-to-one correspondence.

6. The integrated circuit as recited in claim 5, wherein each of said micromachined elements is hexagonal and each of said CMOS cells is rectangular.

7. The integrated circuit as recited in claim 65, wherein each of said micromachined elements comprises at least one capacitive micromachined ultrasonic transducer.

8. The integrated circuit as recited in claim 5, wherein said CMOS cells are arranged in columns, an axis of symmetry of said hexagonal arrangement of micromachined elements being parallel to a column direction.

9. The integrated circuit as recited in claim 8, wherein every other column of said CMOS cells is offset from adjoining columns by a distance equal to one-half of the cell dimension in said column direction, and the width of each cell is selected so that the CMOS cells line up with respective micromachined elements.

10. An integrated circuit comprising:

a substrate comprising a hexagonal arrangement of CMOS cells; and

a hexagonal arrangement of cMUT elements,

wherein each cMUT element overlies a respective CMOS cell in one-to-one correspondence.

11. The integrated circuit as recited in claim 10, wherein each of said cMUT elements is hexagonal and each of said CMOS cells is rectangular.

12. The integrated circuit as recited in claim 10, wherein each of said cMUT elements comprises a respective array of hexagonal cMUT cells having their electrodes hard-wired together.

13. The integrated circuit as recited in claim 10, wherein said CMOS cells are arranged in columns, an axis of symmetry of said hexagonal arrangement of cMUT elements being parallel to a column direction.

14. The integrated circuit as recited in claim 13, wherein every other column of said CMOS cells is offset from adjoining columns by a distance equal to one-half of the cell dimension in said column direction, and the width of each cell is selected do that the CMOS cells line up with respective micromachined elements.